3. The method as defined in claim 6 wherein the implanting dose of the backside p^+ emitter is approximately between $1x10^{11}$ and $1x10^{17}$ cm^{-2}.

4. The method as defined in claim 6 wherein the thickness of the n-type residual diffused-layer contained in the n-type base is approximately between 5 and 50 μm.

5. The method as defined in claim 6 wherein the doping concentration of the n-type residual diffused-layer is in a range of approximately $1x10^{14}$~$1x10^{17}$ cm^{-3} at the interface of the residual layer and the backside p^+ emitter.

6. A method for fabricating low-power-loss power semiconductor switching devices, wherein the fabrication is in the following sequence:

PROCEDURE I: fabricating a nonuniformly doped n-type substrate which contains a diffused n^+ layer on one side, wherein the diffused layer, which is finally near to the backside p^+ emitter, is formed in the first step of this procedure before the thinning of the substrate;

PROCEDURE II: fabricating the general frontside structure of either an IGBT, MCT, or GTO on the low-concentration side of the n-type substrate using ion implanting, high-temperature diffusion and so on;

PROCEDURE III: thinning the wafer from the high-concentration side of the substrate by such commonly used techniques as grinding and polishing, so that the thickness of the residual diffused-layer is decreased to a required value;

PROCEDURE IV: forming the backside p^+ emitter with a required thickness by ion implanting into the surface of the residual diffused-layer;

PROCEDURE V: depositing metals on the surface of the backside p^+ layer, followed by sintering/alloying; and